WHAT IS CLAIMED IS:

1. A method comprising:

serially receiving, from a source, a plurality of forward messages each addressed to one of a plurality of destinations;

receiving a plurality of availability signals, each availability signal indicating that one of the destinations is available to accept a forward message;

simultaneously sending a forward message to each available destination;

simultaneously receiving, after a predetermined period of time, a plurality of reverse messages from the destinations, each reverse message corresponding to one of the forward messages simultaneously sent to an available destination; and

serially sending the reverse messages to the source.

2. The method of claim 1, wherein the source identifies each of the forward messages by a different tag, further comprising:

placing a tag in a delay buffer when sending to a destination the forward message identified by that tag, wherein the delay buffer implements a delay equal to the predetermined period of time such that the tag is available when receiving from memory the reverse message corresponding to the forward message; and

sending the tag to the source with the reverse message, whereby the source associates the reverse message with the forward message.

3. The method of claim 1, further comprising:

associating a priority with each forward message; and

sending a forward message to a destination when that forward message has a higher priority than other forward messages addressed to that destination.

4. The method of claim 3, wherein the priority of each forward message represents an age of that forward message.

5. The method of claim 1, further comprising:

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associating a priority with each reverse message; and

sending a forward message to the source when that reverse message has a higher priority than other reverse messages.

6. The method of claim 5, wherein the priority of each reverse message represents an age of that reverse message.

7. The method of claim 1, wherein each destination is a memory bank, each forward message is a memory transaction, and each reverse message is the result of one of the memory transactions.

8. An apparatus comprising:

means for serially receiving, from a source, a plurality of forward messages each addressed to one of a plurality of destinations;

means for receiving a plurality of availability signals, each availability signal indicating that one of the destinations is available to accept a forward message;

means for simultaneously sending a forward message to each available destination;

means for simultaneously receiving, after a predetermined period of time, a plurality of reverse messages from the destinations, each reverse message corresponding to one of the forward messages simultaneously sent to an available destination; and

means for serially sending the reverse messages to the source.

9. The apparatus of claim 8, wherein the source identifies each of the forward messages by a different tag, further comprising:

means for placing a tag in a delay buffer when sending to a destination the forward message identified by that tag, wherein the delay buffer implements a delay equal to the predetermined period of time such that the tag is available when receiving from memory the reverse message corresponding to the forward message; and

means for sending the tag to the source with the reverse message, whereby the source associates the reverse message with the forward message.

10. The apparatus of claim 8, further comprising:

means for associating a priority with each forward message; and

means for sending a forward message to a destination when that forward message has a higher priority than other forward messages addressed to that destination.

11. The apparatus of claim 10, wherein the priority of each forward message represents an age of that forward message.

12. The apparatus of claim 8, further comprising:

means for associating a priority with each reverse message; and

means for sending a forward message to the source when that reverse message has a higher priority than other reverse messages.

13. The apparatus of claim 12, wherein the priority of each reverse message represents an age of that reverse message.

14. The apparatus of claim 8, wherein each destination is a memory bank, each forward message is a memory transaction, and each reverse message is the result of one of the memory transactions.

15. A computer program product, tangibly stored on a computer-readable medium, comprising instructions operable to cause a programmable processor to:

serially receive, from a source, a plurality of forward messages each addressed to one of a plurality of destinations;

receive a plurality of availability signals, each availability signal indicating that one of the destinations is available to accept a forward message;

simultaneously send a forward message to each available destination;

simultaneously receive, after a predetermined period of time, a plurality of reverse messages from the destinations, each reverse message corresponding to one of the forward messages simultaneously sent to an available destination; and

serially send the reverse messages to the source.

16. The computer program product of claim 15, wherein the source identifies each of the forward messages by a different tag, further comprising instructions operable to cause a programmable processor to:

place a tag in a delay buffer when sending to a destination the forward message identified by that tag, wherein the delay buffer implements a delay equal to the predetermined period of time such that the tag is available when receiving from memory the reverse message corresponding to the forward message; and

send the tag to the source with the reverse message, whereby the source associates the reverse message with the forward message.

17. The computer program product of claim 15, further comprising instructions operable to cause a programmable processor to:

associate a priority with each forward message; and

send a forward message to a destination when that forward message has a higher priority than other forward messages addressed to that destination.

18. The computer program product of claim 17, wherein the priority of each forward message represents an age of that forward message.

19. The computer program product of claim 15, further comprising instructions operable to cause a programmable processor to:

associate a priority with each reverse message; and

send a forward message to the source when that reverse message has a higher priority than other reverse messages.

20. The computer program product of claim 19, wherein the priority of each reverse message represents an age of that reverse message.

21. The computer program product of claim 15, wherein each destination is a memory bank, each forward message is a memory transaction, and each reverse message is the result of one of the memory transactions.

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